

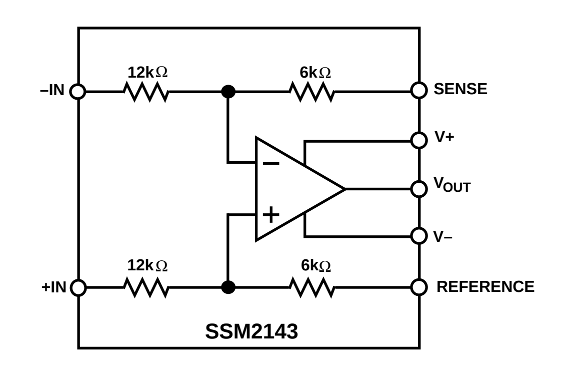
–6 dB Differential Line Receiver

SSM2143

FEATURES
High Common-Mode Rejection
- **DC: 90 dB typ**
- **60 Hz: 90 dB typ**
- **20 kHz: 85 dB typ**

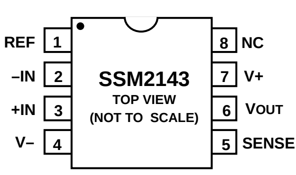
Ultralow THD: 0.0006% typ @ 1 kHz
Fast Slew Rate: 10 V/µs typ
Wide Bandwidth: 7 MHz typ (G = 1/2)
Two Gain Levels Available: G = 1/2 or 2
Low Cost

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS

**Epoxy Mini-DIP (P Suffix)
and
SOIC (S Suffix)**



NC = NO CONNECT

GENERAL DESCRIPTION

The SSM2143 is an integrated differential amplifier intended to receive balanced line inputs in audio applications requiring a high level of immunity from common-mode noise. The device provides a typical 90 dB of common-mode rejection (CMR), which is achieved by laser trimming of resistances to better than 0.005%.

Additional features of the device include a slew rate of 10 V/µs and wide bandwidth. Total harmonic distortion (THD) is less than 0.004% over the full audio band, even while driving low impedance loads. The SSM2143 input stage is designed to handle input signals as large as +28 dBu at G = 1/2. Although primarily intended for G = 1/2 applications, a gain of 2 can be realized by reversing the +IN/–IN and SENSE/REFERENCE connections.

When configured for a gain of 1/2, the SSM2143 and SSM2142 Balanced Line Driver provide a fully integrated, unity gain solution to driving audio signals over long cable runs. For similar performance with G = 1, see SSM2141.

REV. 0

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Tel: 617/329-4700 Fax: 617/326-8703

SSM2143–SPECIFICATIONS
(V_S = ±15 V, –40°C ≤ T_A ≤ +85°C, G = 1/2, unless otherwise noted. Typical specifications apply at T_A = +25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD+N	V_{IN} = 10 V rms, R_L = 10 kΩ, f = 1 kHz		0.0006		%
Signal-to-Noise Ratio	SNR	0 dBu = 0.775 V rms, 20 kHz BW, RTI		–107.3		dBu
Headroom	HR	Clip Point = 1% THD+N		+28.0		dBu
DYNAMIC RESPONSE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 200 pF	6	10		V/µs
Small Signal Bandwidth	$BW_{-3\ dB}$	R_L = 2 kΩ, C_L = 200 pF				
		G = 1/2		7		MHz
		G = 2		3.5		MHz
INPUT						
Input Offset Voltage	V_{IOS}	V_{CM} = 0 V, RTI, G = 2	–1.2	0.05	+1.2	mV
Common-Mode Rejection	CMR	V_{CM} = ±10 V, RTO				
		f = dc	70	90		dB
		f = 60 Hz		90		dB
		f = 20 kHz		85		dB
		f = 400 kHz		60		dB
Power Supply Rejection	PSR	V_S = ±6 V to ±18 V	90	110		dB
Input Voltage Range	IVR	Common Mode		±15		V
		Differential		±28		V
OUTPUT						
Output Voltage Swing	V_O	R_L = 2 kΩ	±13	±14		V
Minimum Resistive Load Drive				2		kΩ
Maximum Capacitive Load Drive				300		pF
Short Circuit Current Limit	I_{SC}			+45, –20		mA
GAIN						
Gain Accuracy			–0.1	0.03	0.1	%
REFERENCE INPUT						
Input Resistance				18		kΩ
Voltage Range				±10		V
POWER SUPPLY						
Supply Voltage Range	V_S		±6		±18	V
Supply Current	I_{SY}	V_{CM} = 0 V, R_L = ∞		±2.7	±4.0	mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . ±18 V
Common-Mode Input Voltage . . . . ±22 V
Differential Input Voltage . . . . ±44 V
Output Short Circuit Duration . . . . Continuous
Operating Temperature Range . . . . –40°C to +85°C
Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . +150°C
Lead Temperature (Soldering, 60 sec) . . . . +300°C
Thermal Resistance
  8-Pin Plastic DIP (P): θ_{JA} = 103, θ_{JC} = 43 . . . . °C/W
  8-Pin SOIC (S): θ_{JA} = 150, θ_{JC} = 43. . . . . °C/W

ORDERING GUIDE

Model	Operating Temperature Range	Package Description	Package Option
SSM2143P	–40°C to +85°C	8-Pin Plastic DIP	N-8
SSM2143S*	–40°C to +85°C	8-Pin SOIC	SO-8

*Contact sales office for availability.

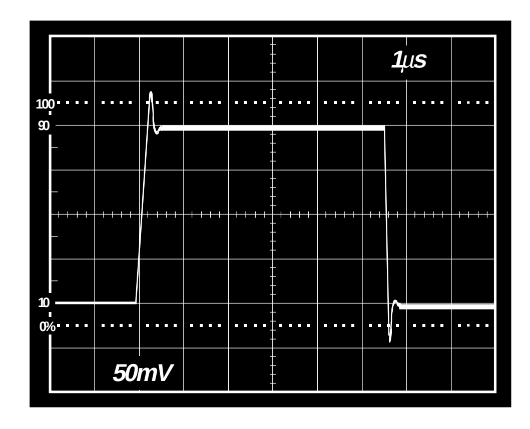


Figure 1. Small-Signal Transient Response (V_{IN} = ±200 mV, G = 1/2, R_L = 2 kΩ, V_S = ±15 V, T_A = +25°C)

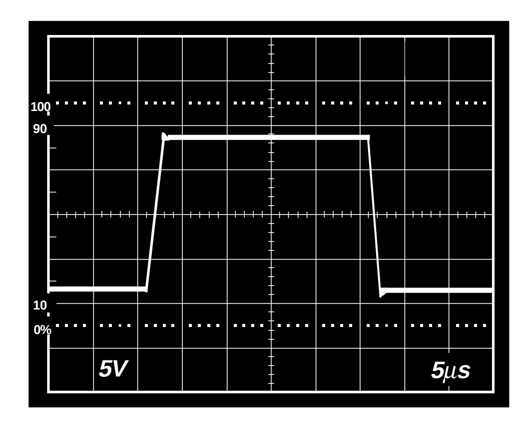


Figure 2. Large Signal Transient Response (V_{IN} = +24 dBu, G = 1/2, R_L = 2 kΩ V_S = ±15 V, T_A = +25°C)

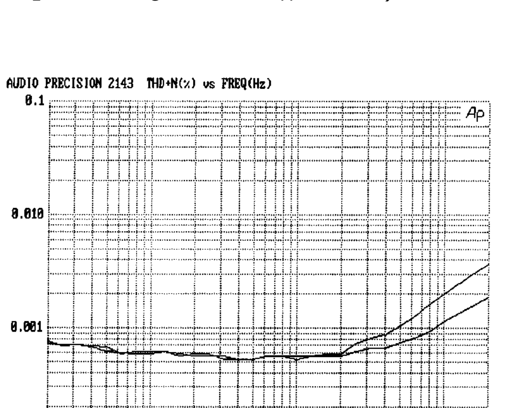


Figure 3. THD+N vs. Frequency (V_S = ±15 V, V_{IN} = 10 V rms, with 80 kHz Filter)

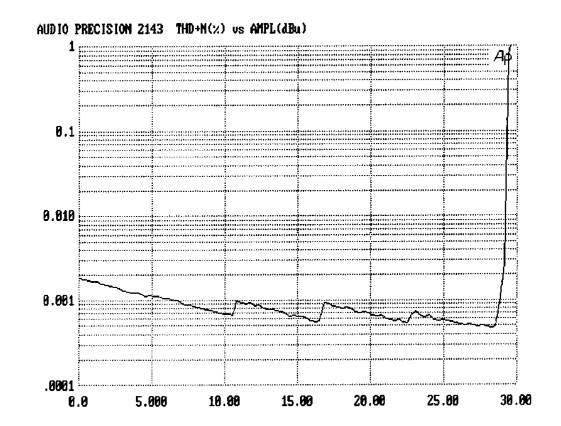


Figure 4. Headroom (V_S = ±15 V, R_L = 10 kΩ, with 80 kHz Filter)

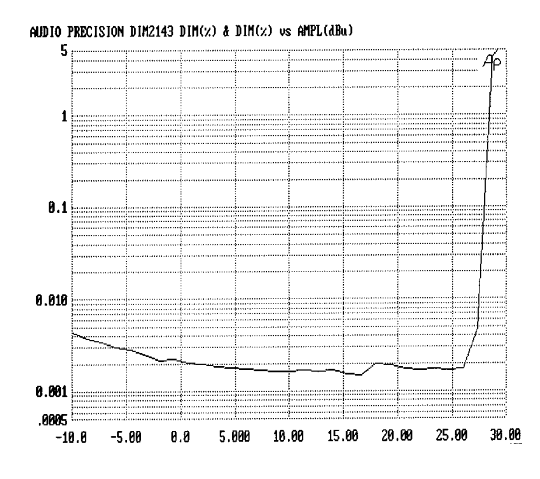


Figure 5. Dynamic Intermodulation Distortion, DIM-100 (V_S = ±15 V, R_L = 100 kΩ)

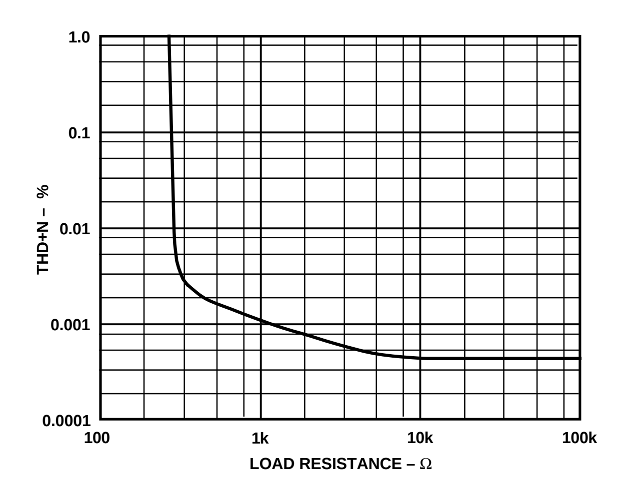


Figure 6. THD+N vs. Load (V_S = ±15 V, V_{IN} = 10 V rms, with 1 kHz Sine, 80 kHz Filter)

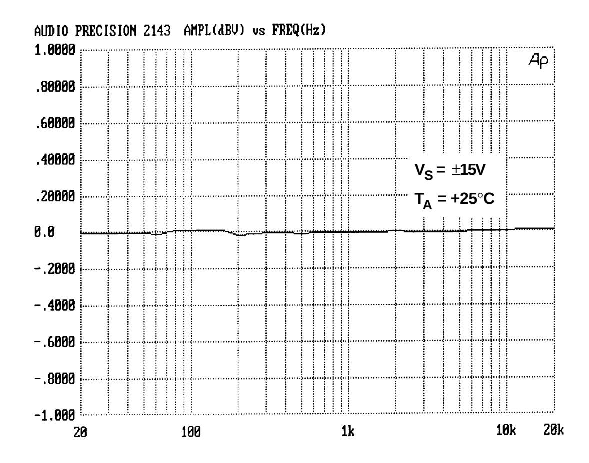


Figure 7. Closed-Loop Gain vs. Frequency, 20 Hz to 20 kHz (Gain of 1/2 Normalized to 0 dB)

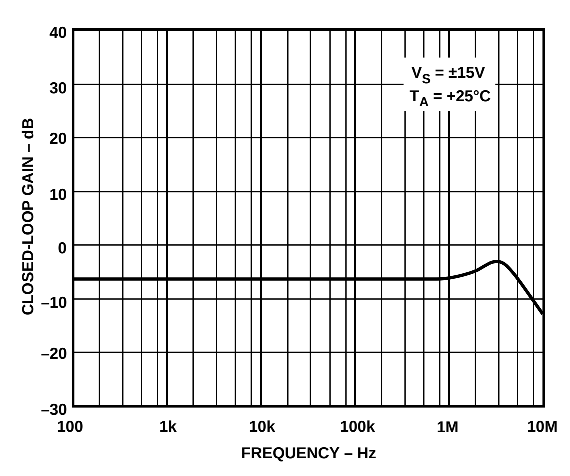


Figure 8. Closed-Loop Gain vs. Frequency, 100 Hz to 10 MHz

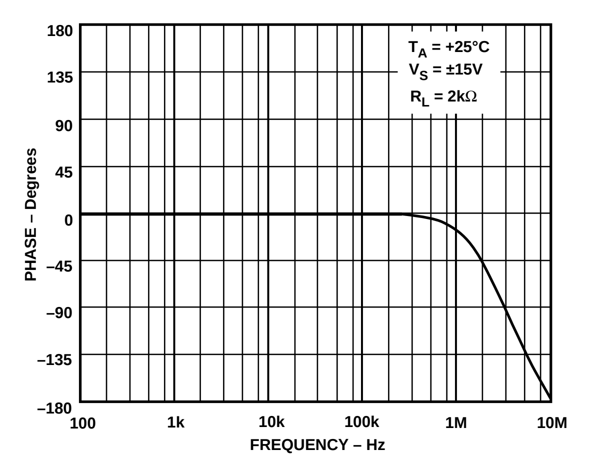


Figure 9. Closed-Loop Phase vs. Frequency

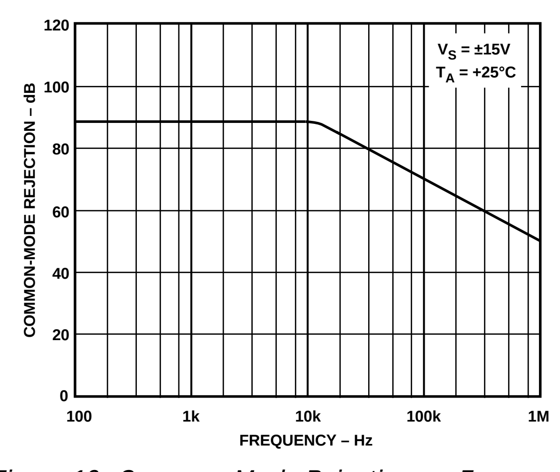


Figure 10. Common-Mode Rejection vs. Frequency

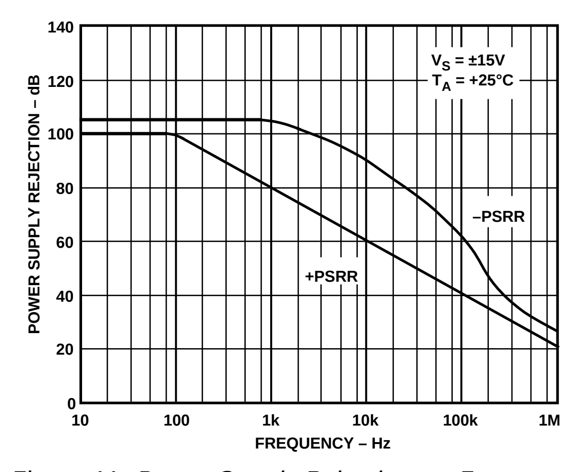


Figure 11. Power Supply Rejection vs. Frequency

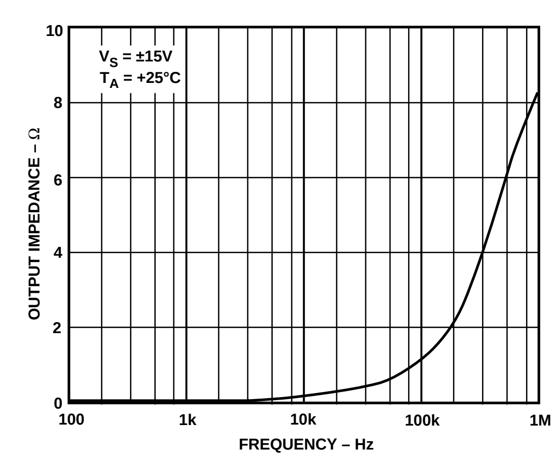


Figure 12. Closed-Loop Output Impedance vs. Frequency

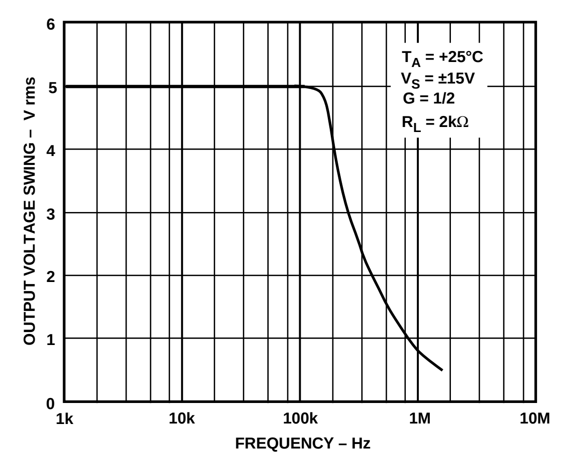


Figure 13. Output Voltage Swing vs. Frequency

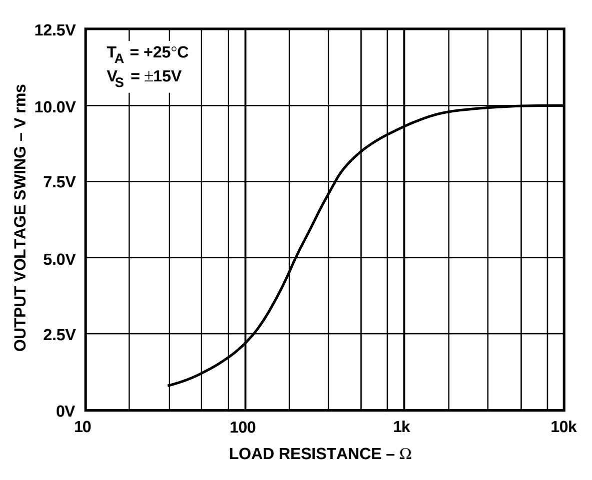


Figure 14. Output Voltage Swing vs. Load Resistance

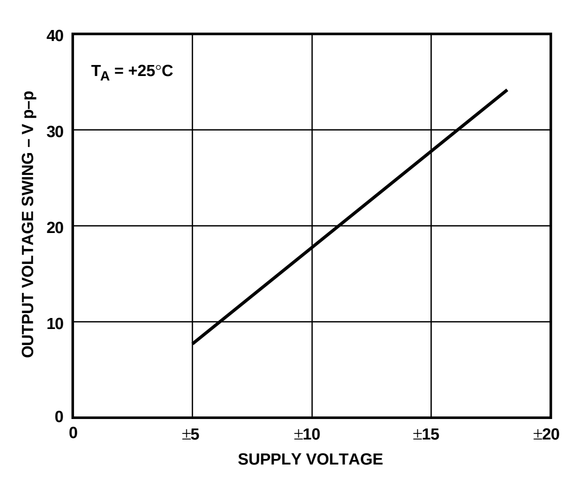


Figure 15. Output Voltage Swing vs. Supply Voltage

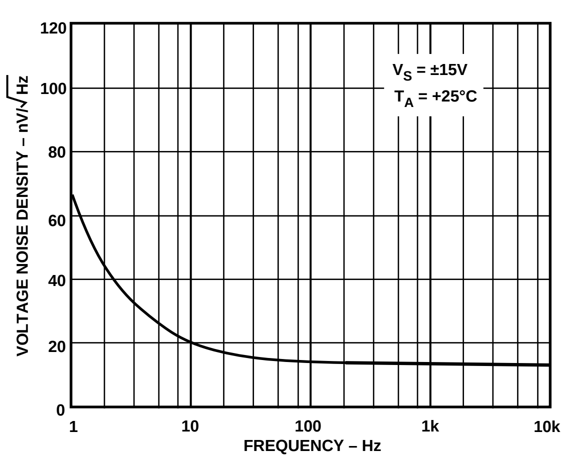


Figure 16. Voltage Noise Density vs. Frequency

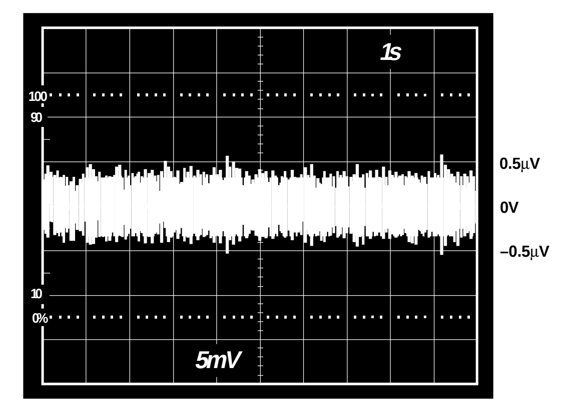


*Figure 17. Low Frequency Voltage Noise from 0.1 Hz to 10 Hz**

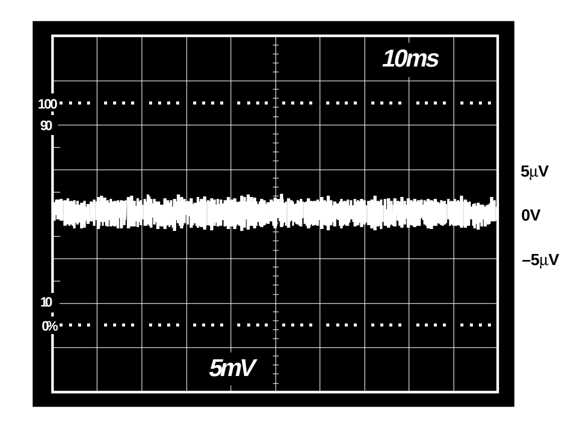


*Figure 18. Voltage Noise from 0 kHz to 1 kHz**

*The photographs in Figure 17 through Figure 19 were taken at V_S = ±15 V and T_A = +25°C, using an external amplifier with a gain of 1000.

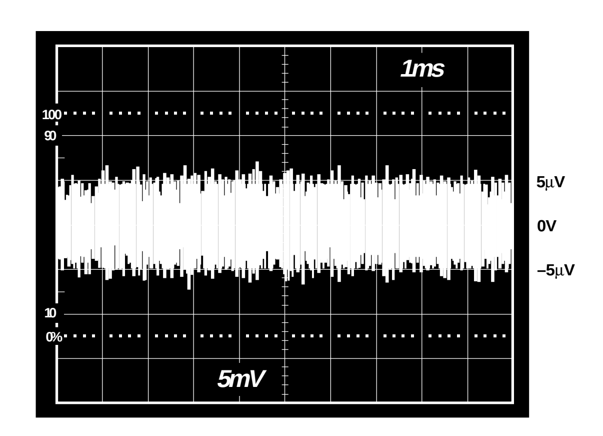


Figure 19. Voltage Noise from 0 kHz to 10 kHz*

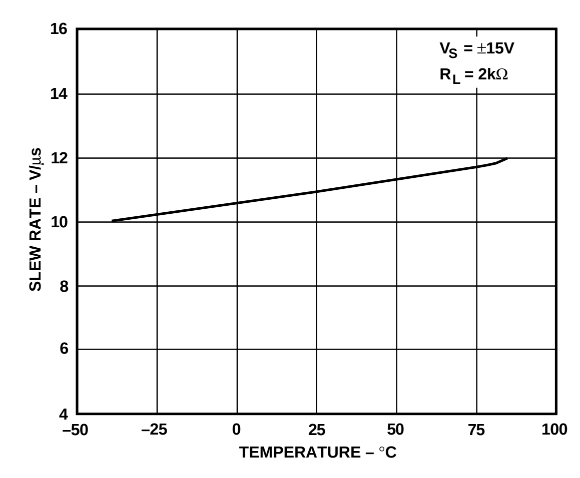


Figure 20. Slew Rate vs. Temperature

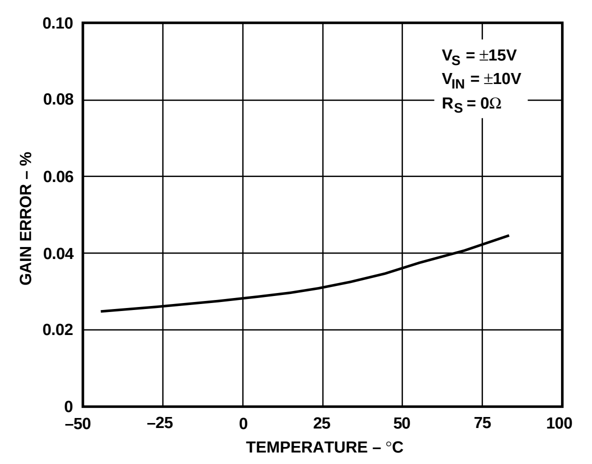


Figure 21. Gain Error vs. Temperature

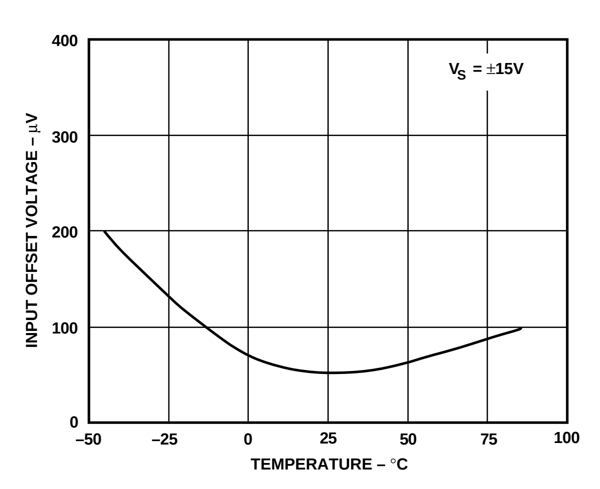


Figure 22. Input Offset Voltage vs. Temperature

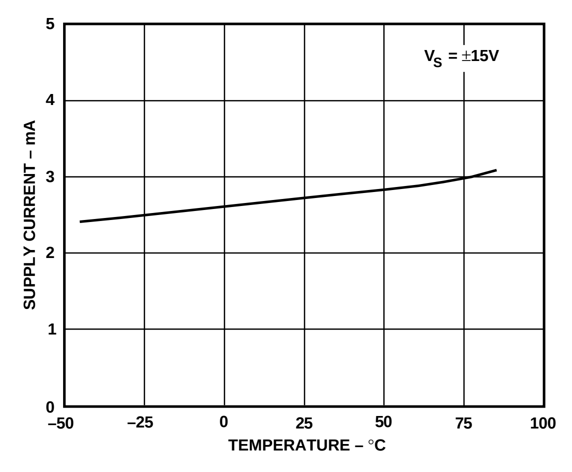


Figure 23. Supply Current vs. Temperature

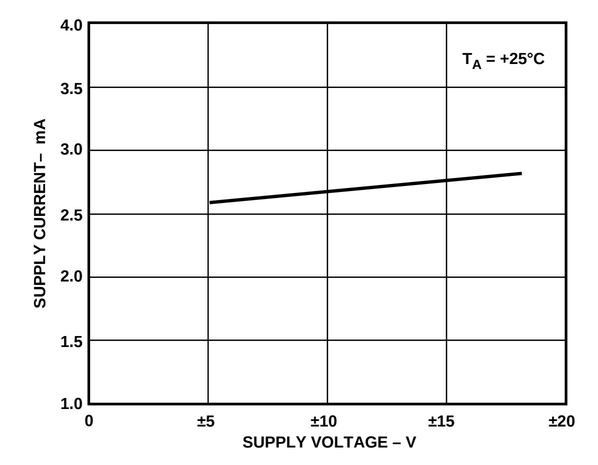


Figure 24. Supply Current vs. Supply Voltage

*The photographs in Figure 17 through Figure 19 were taken at V_S = ±15 V and T_A = +25°C, using an external amplifier with a gain of 1000.

APPLICATIONS INFORMATION

The SSM2143 is designed as a balanced differential line receiver. It uses a high speed, low noise audio amplifier with four precision thin-film resistors to maintain excellent common-mode rejection and ultralow THD. Figure 25 shows the basic differential receiver application where the SSM2143 yields a gain of 1/2. The placement of the input and feedback resistors can be switched to achieve a gain of +2, as shown in Figure 26. For either circuit configuration, the SSM2143 can also be used unbalanced by grounding one of the inputs. In applications requiring a gain of +1, use the SSM2141.

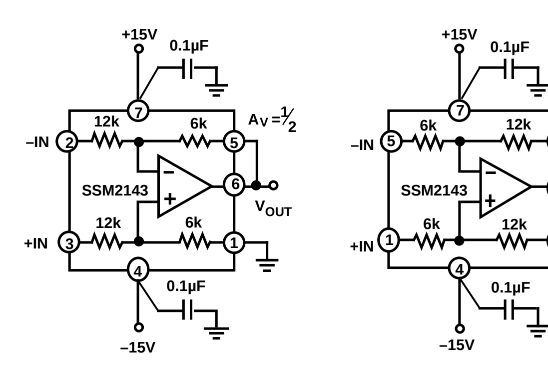


Figure 25. Standard Configuration for Gain of 1/2

Figure 26. Reversing the Resistors Results in a Gain of 2

CMRR

The internal thin-film resistors are precisely trimmed to achieve a CMRR of 90 dB. Any imbalances introduced by the external circuitry will cause a significant reduction in the overall CMRR performance. For example, a 5 Ω source imbalance will result in a CMRR of 71 dB at dc. This is also true for any reactive source impedances that may affect the CMRR over the audio frequency range. These error sources need to be minimized to maintain the excellent CMRR.

To quantify the required accuracy of the thin film resistor matching, the source of CMRR error can be analyzed. A resistor mismatch can be modelled as shown in Figure 27. By assuming a tolerance on one of the 12 kΩ resistors of ΔR, the equation for the common-mode gain becomes:

$$\frac{V_{OUT}}{V_{IN}} = \frac{6k}{6k+12k}\left(\frac{6k}{12k+\Delta R}+1\right) - \frac{6k}{12k+\Delta R}$$

which reduces to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1/3\,\Delta R}{12k+\Delta R}$$

This gain error leads to a common-mode rejection ratio of:

$$CMRR = \frac{|A_{DM}|}{|A_{CM}|} \cong \frac{18k}{\Delta R}$$

Figure 27. A Small Mismatch in Resistance Results in a Large Common-Mode Error

Setting ΔR to 5 Ω results in the CMRR of 71 dB, as stated above. To achieve the SSM2143's CMRR of 90 dB, the resistor mismatch can be at most 0.57 Ω. In other words, to build this circuit discretely, the resistors would have to be matched to better than 0.005%!

The following table shows typical resistor accuracies and the resulting CMRR for a differential amplifier.

% Mismatch	CMRR
5%	30 dB
1%	44 dB
0.1%	64 dB
0.005%	90 dB

DC OUTPUT LEVEL ADJUST

The reference node of the SSM2143 is normally connected to ground. However, it can be used to null out any dc offsets in the system or to introduce a dc reference level other than ground. As shown in Figure 28, the reference node needs to be

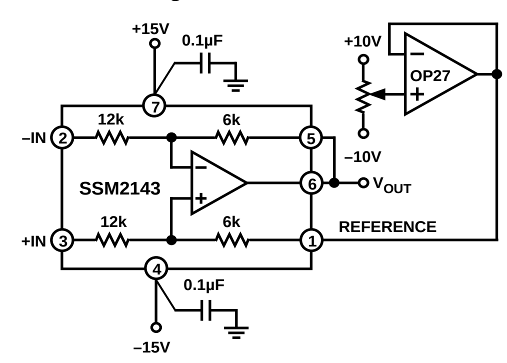


Figure 28. A Low Impedance Buffer Is Required to Adjust the Reference Voltage.

buffered with an op amp to maintain very low impedance to achieve high CMRR. The same reasoning as above applies such that the 6 kΩ resistor has to be matched to better than 0.005% or 0.3 Ω. The op amp maintains very low output impedance over the entire audio frequency range, as long as its bandwidth is well above 20 kHz. The reference input can be adjusted over a ±10 V range. The gain from the reference to the output is unity so the resulting dc output adjustment range is also ±10 V.

INPUT ERRORS

The main dc input offset error specified for the SSM2143 is the Input Offset Voltage. The Input Bias Current and Input Offset Current are not specified as for a normal operational amplifier. Because the SSM2143 has built-in resistors, any bias current related errors are converted into offset voltage errors. Thus, the offset voltage specification is a combination of the amplifier's offset voltage plus its offset current times the input impedance.

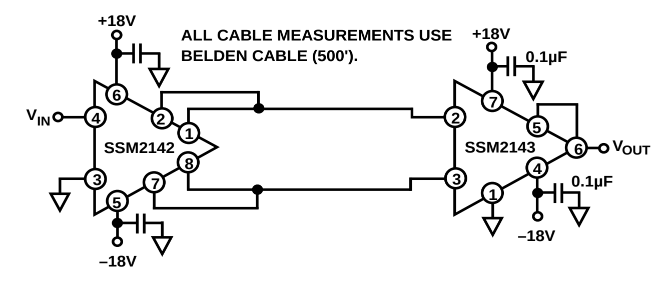


Figure 29. SSM2142/SSM2143 Balanced Line Driver/Receiver System

LINE DRIVER/RECEIVER SYSTEM

The SSM2143 and SSM2142 provide a fully integrated line driver/receiver system. The SSM2142 is a high performance balanced line driver IC that converts an unbalanced input into a balanced output signal. It can drive large capacitive loads on long cables making it ideal for transmitting balanced audio signals. When combined with an SSM2143 on the receiving end of the cable, the system maintains high common-mode rejection and ultralow THD. The SSM2142 is designed with a gain of +2 and the SSM2143 with a gain of 1/2, providing an overall system gain of unity.

The following data demonstrates the typical performance of the two parts together, measured on an Audio Precision at the SSM2143's output. This configuration was tested with 500 feet of cable between the ICs as well as no cable. The combination of the two parts results in excellent THD+N and SNR and a noise floor of typically –105 dB over a 20 Hz to 20 kHz bandwidth.

A comment on SSM2142/SSM2143 system headroom is necessary. Figure 31 shows a maximum signal handling of approximately ±22 dBu, but it must be kept in mind that this is measured between the SSM2142's input and SSM2143's output, which has been attenuated by one half. Normally, the system would be shown as actually used in a piece of equipment, whereby the SSM2143 is at the input and SSM2142 at the output. In this case, the system could handle differential signals in excess of +24 dBu at the input and output, which is consistent with headroom requirements of most professional audio equipment.

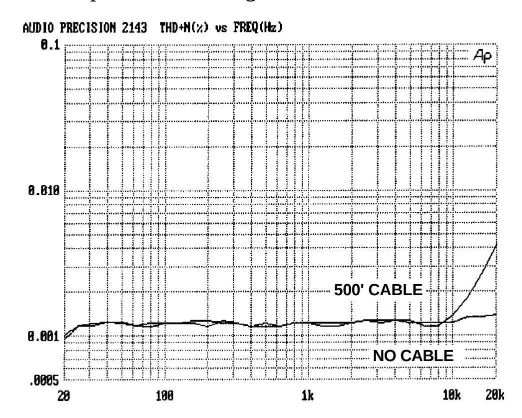


Figure 30. THD+N vs. Frequency of SSM2142/SSM2143 System (V_S = ±18 V, V_{IN} = 5 V rms, with 80 kHz Filter)

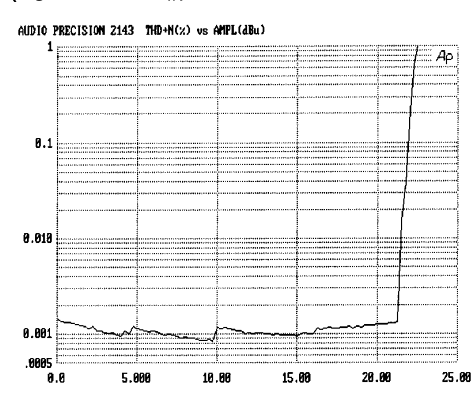


Figure 31. SSM2142/SSM2143 System Headroom–See Text—(V_S = ±18 V, R_L = 10 kΩ, 500' Cable)

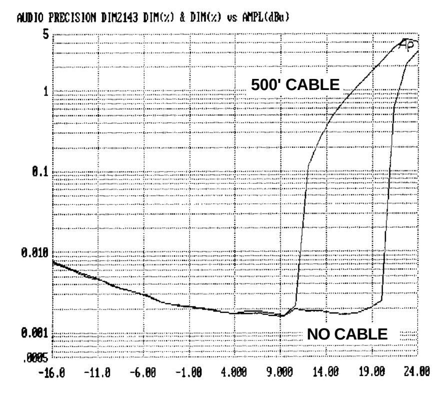


Figure 32. SSM2142/SSM2143 System DIM-100 Dynamic Intermodulation Distortion (V_S = ±18 V, R_L = 10 kΩ)

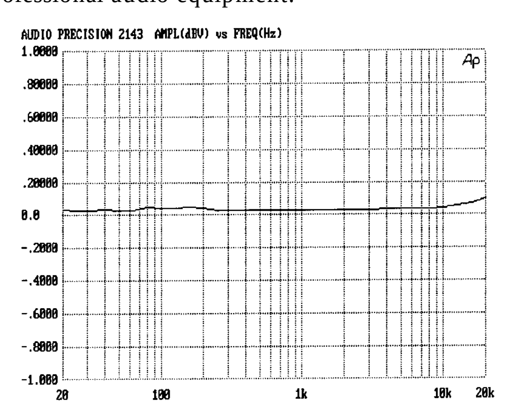


Figure 33. SSM2142/SSM2143 System Frequency Response (V_S = ±18 V, V_{IN} = 0 dBV, 500' Cable)

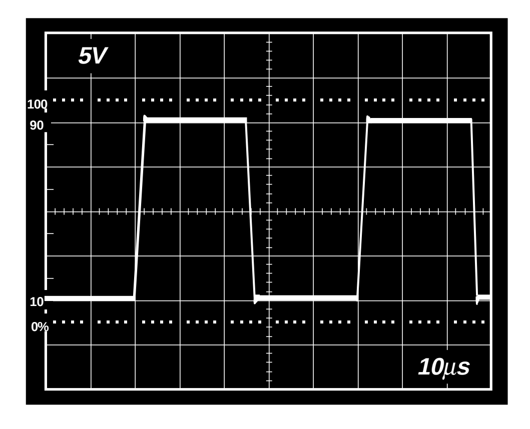
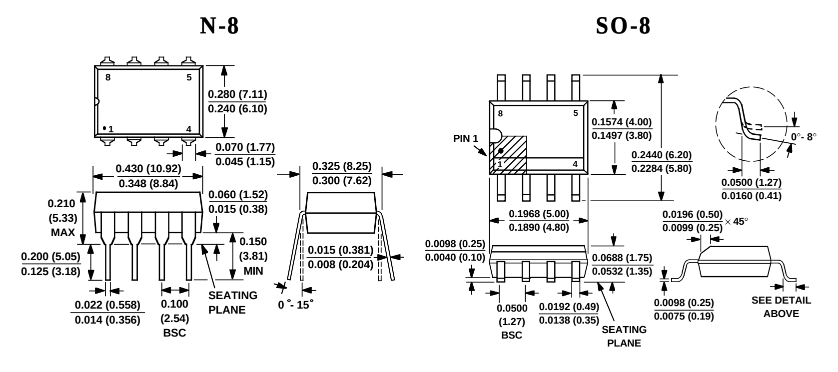


Figure 34. SSM2142/SSM2143 System Large Signal Pulse Response (V_S = ±18 V, R_L = 10 kΩ, No Cable)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

N-8 **SO-8**



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